

### **Board Bring Up** Introduction

### Emil Damkjaer Petersen

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- 2 Hardware Selection
- 3 Board Bring-Up



### Goal of this presentation

- Provide information to help developers with selecting hardware for graphcis applications
  - Preleminary considerations for how the application can have an impact on the needed hardware
  - Information on the hardware components that an embedded GUI solution consist of
- Guide developers in the Board Bring Up phase, thereby helping with setting up the neccesary parts for an GUI solution and ensuring the drivers work





### Further reading

- More help and information can be found at the TouchGFX documentation site: <u>https://support.touchgfx.com/</u>
- Slides in this presentation will refer to relevant documentation pages. Links will be in the lower right-hand corner of the slides
- The presentation will general be related to the two sections: <u>Hardware Selection & Board Bring Up</u>



### TouchGFX Development Main Activies Main Component Display Board Bring Up Display TouchGFX AL Development Display TouchGFX AL Display Display TouchGFX AL Display Display TouchGFX AL Display

This presentation will start out with discussing the Main Activty, Hardware Selection, before it moves on to the activity Board Bring Up. Thereby we will learn how to select the hardware components needed for the Display Board, before moving on to the initialization of the selected hardware compnents, as a part of the Board Initialization Code, Main Component.



6



- Preliminary Considerations
  - Application design have impact on the hardware
    - Display Resolution
    - Color Depth
    - Animations
    - Complexity
    - Size
    - Touch
  - Mechanical Design Requirements
    - Size
    - Environment



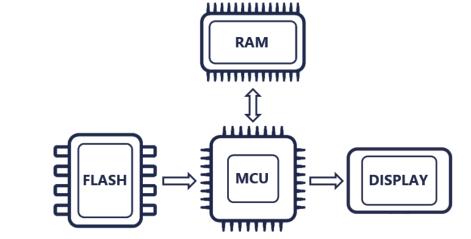




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- The basic hardware can be divided into 4 parts
  - MCU
    - Heavy Lifting
  - RAM
    - Framebuffer
  - Flash
    - Images, Fonts, Texts
  - Display



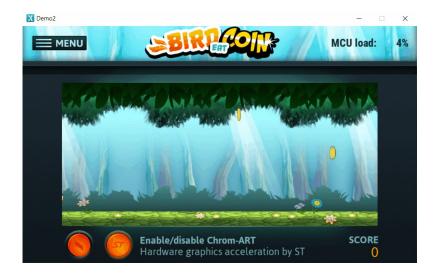


• More information can be found in the documentation:

Hardware Selection

### **MCU PORTFOLIO FOR GRAPHICS**

			Г Т	
STM32 SERIES	FREQUENCY	HARDWARE ACCELERATION	DISPLAY INTERFACES	SUPPORTED RESOLUTIONS
STM32G0 (CM0+)	64 MHz		SPI	Up to 320*240
STM32F7 (CM7)	216 MHz	Chrom-ART ™ Hardware JPEG Codec	Parallel LCD TFT MIPI-DSI	Up to 1024*768



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### • MCU

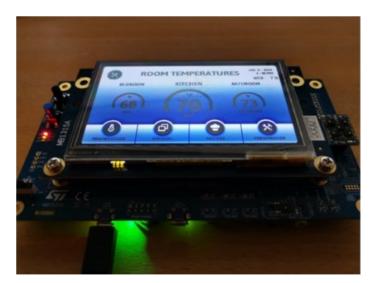
- Frequency
- Embedded Hardware Acceleration
  - Chrom-ART
  - JPEG Accelerator
  - Chrom-GRC
- Internal Memory
  - Ram
  - Flash
- LCD Controller
- Packages & I/O
- Memory Interfacing





- Display
  - Different Types of Display
    - LCD-TFT
    - MIP
    - ePaper/elnk
  - Display Interface
  - Brightness and Backlight
  - Viewing Position and Color Inversion
  - Pixel density
  - Displays with RAM
  - Environment



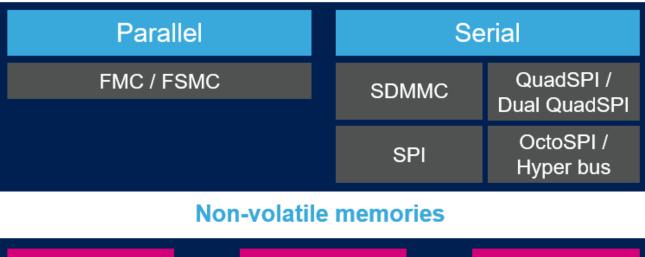






- External Memory
  - MCU memory interface
  - Non-volatile Memories
    - NOR Flash
    - NAND Flash
    - eMMC
  - Volatile Memories
    - SDRAM
    - SRAM
    - PSRAM

### **MCU** memory interfaces









- Introduction
  - Tools of the trade
    - STM32CubeMX
    - STM32Cube Firmware Package
    - Vendor datasheets
    - Vendor driver code
  - Verification of Functionality
    - Abstraction Layer
    - Test Code







- Introduction
  - How To Guide
    - Motivation
    - Goal
    - Prerequisites
    - Do

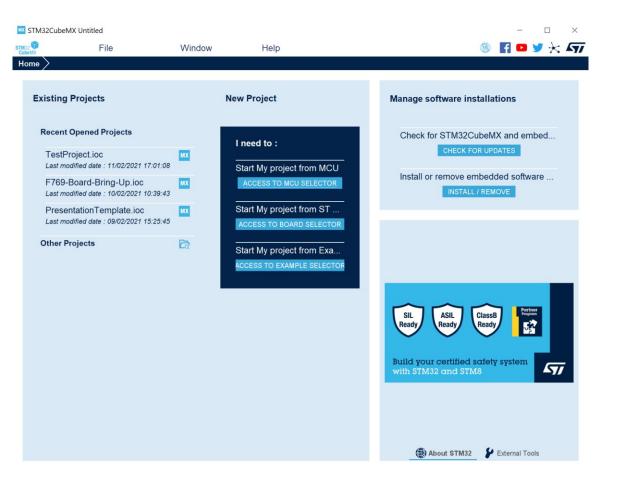
Step	Content
Create Project	Create an empty project in CubeMX
CPU Running	Ensure that the MCU is running at the desired speed
Framebuffer in internal RAM	Allocate a framebuffer in internal RAM and transmit it to the display
External RAM	Enable the external RAM
Framebuffer in external RAM	Move the framebuffer to external RAM and transmit it to the display
External addressable flash	Enable external memory-mapped flash
External block mode flash	Enable external block-mode flash
Hardware acceleration	Enable the Chrom-ART graphics accelerator
Touch controller	Setup communication to the touch controller
Physical buttons	Configure access to physical buttons
Flash loader	Develop a way to write data to the external flash



- 1. Create Project
  - Motivation
    - Have a project in the chosen IDE and STM32CubeMX to be the basis for board bring up
  - Goal

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- Working STM32CubeMX project
- Able to debug code on the MCU
- Prerequisites
  - STM32 Based Board
  - Programming/Debugging interface
  - STM32CubeMX
  - IDE Installed



- 1. Create Project
  - Do
    - Create a project in STM32CubeMX based on the MCU on the Board
    - Select "Advance" under application structure, and don't select "Do not generate the main()"
    - Select Toolchain/IDE
    - Generate Code and when done, open project
    - Compile and debug from IDE

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U/MPU Filters							
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Series	>	STM32F769	N	r, L1 cache,		MIPI-DSI, JPE	
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Package	>	ACTIVE Acti Product is in mar	ve			TFBGA216	
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- 1. Create Project
  - Do
    - Create a project in STM32CubeMX based on the MCU on the Board
    - Select "Advance" under application structure, and don't select "Do not generate the main()"
    - Select Toolchain /IDE
    - Generate Code and when done, open project
    - Compile and debug from IDE

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	File	Window	Help	🧐	🖸 🄰 🔆 🏹
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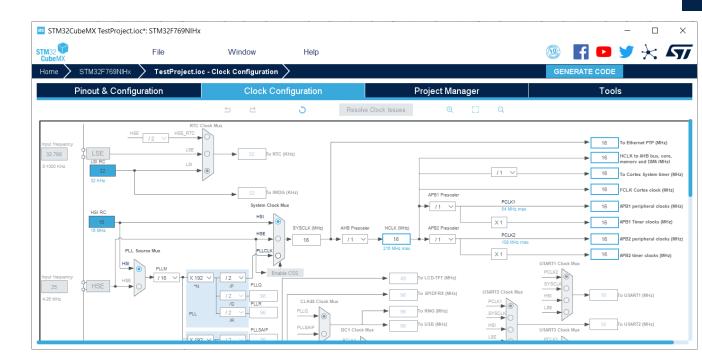
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ebug Log		<b>▼</b> ₽ 3
Log Thu Feb 11, 2021 14:28:35: Hardware re Thu Feb 11, 2021 14:28:35: Target rese	set with strategy 0 was performed	^ ^ •



### • 2. CPU Running

- Motivation
  - Ensure that the MCU core, Internal RAM and flash is running a desired clock speed
- Goal
  - Set up clock to ensure correct speed
- Prerequisites
  - Information about clock on hardware
- Do
  - Setup clock in STM32CubeMX under the Clock Configuration
  - Check speed by debugging
- Note





	51	
	92	/* Infinite loop */
	93	/* USER CODE BEGIN WHILE */
	94	HAL Delay(5000);
•	95	while (1)
	96 🚍	{
	97	/* USER CODE END WHILE */
	99	

#### How To: 2. CPU Running 21

### **Board Bring Up**

### • 2. CPU Running

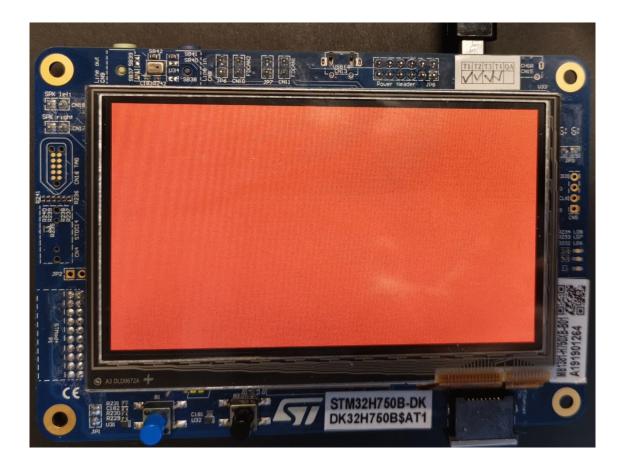
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  - Check speed by debugging
- Note



45	/* USER CODE BEGIN PV */	
46	<pre>volatile uint32_t result;</pre>	
47	<pre>volatile uint32_t time;</pre>	
48	/* USER CODE END PV */	

	97	uint32_t* code = (uint32_t*)0x08000000;
	98	uint32_t* stop = (uint32_t*)0x08020000;
	99	uint32_t sum = 0;
	100	
	01	uint32_t start = HAL GetTick();
	102	
	103	while (code != stop)
	104 🚍	{
	105	<pre>sum += *code++;</pre>
	106 -	}
	107	result = sum;
	108	uint32_t end = HAL_GetTick();
	109	time = end - start;
	110	
ack	<b>G</b> 111	while (1)
JUK	112 🛱	{
	113	/* HEED CONE END WUTTE */

- 3. Framebuffer in internal RAM
  - Motivation
    - Setting up an internal framebuffer and the display, enables us to have simple graphic on the display
  - Goal
    - Having internal RAM allocated for the framebuffer, and show it's content on the display
  - Prerequisites
    - Information about the Display
    - Information about connection between the MCU and Display





### • 3. Framebuffer in internal RAM

- Do
  - Parallel RGB Displays
    - Setup framebuffer in internal RAM
    - Configure the GPIO connections to the display
    - Configure the LTDC controller
    - Configure the LTDC pixel clock
    - Setting the framebuffer address
    - Check the framerate

main.c

#### uint16\_t framebuffer[480\*272]; //16 bpp framebuffer

~	· ©					nd Configuration			
ategories A->Z					N	lode			
System Core	>	Display Type RGB	888 (24 bits)						~
System Core									
Analog	>								
Timers	>								
Connectivity	>				Confi	guration			
Multimedia	~	Reset Configuration			00111	guiation			
		😔 Parameter Setting	s 😔 Layer Settings	😔 User Constants 🛛 🤇	🕗 NVIC Settings 🛛 😔 GF	PIO Settings			
V DMA2D									
HDMI_CEC		Search Signals						_	
Ø 12S1 Ø 12S2		Search (CrtH+F)							Show only Modified
Ø 1252 Ø 1253		Pin Name	Signal on Pin 🗢	GPIO output level	GPIO mode	GPIO Pull-up/Pull-down	Maximum output speed	User Label	Modified
V LTDC		PE4	LTDC B0	n/a		No pull-up and no pull		LCD B0 [RK043FN48	~
Ø SAI1	_	PJ13	LTDC B1	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B1 [RK043FN48	<b>~</b>
A SAI2		PJ14	LTDC B2	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B2 [RK043FN48	<b>~</b>
SPDIFRX		PJ15	LTDC B3	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B3 [RK043FN48	<b>~</b>
		PG12	LTDC B4	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B4 [RK043FN48	<b>~</b>
		PK4	LTDC B5	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B5 [RK043FN48	<b>~</b>
Security	>	PK5	LTDC B6	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B6 [RK043FN48	<b>~</b>
		PK6	LTDC B7	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD B7 [RK043FN48	<b>~</b>
Computing	>	PI14	LTDC CLK	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD CLK [RK043FN4	<b>~</b>
		PK7	LTDC DE	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_DE [RK043FN48	<b>~</b>
Middleware	>	PJ7	LTDC_G0	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G0 [RK043FN48	<b>~</b>
		PJ8	LTDC_G1	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G1 [RK043FN48	<b>~</b>
Application	>	PJ9	LTDC_G2	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G2 [RK043FN48	<b>~</b>
		PJ10	LTDC_G3	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G3 [RK043FN48	<b>~</b>
		PJ11	LTDC_G4	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G4 [RK043FN48	<b>~</b>
		PK0	LTDC_G5	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G5 [RK043FN48	<b>~</b>
		PK1	LTDC_G6	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G6 [RK043FN48	<b>~</b>
		PK2	LTDC_G7	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_G7 [RK043FN48	<b>~</b>
		PI10	LTDC_HSYNC	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_HSYNC [RK043F	<b>~</b>
		PI15	LTDC_R0	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_R0 [RK043FN48	<b>V</b>
		PJ0	LTDC_R1	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_R1 [RK043FN48	<b>V</b>
		PJ1	LTDC_R2	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_R2 [RK043FN48	<b>V</b>
		PJ2	LTDC_R3	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_R3 [RK043FN48	<b>V</b>
		PJ3	LTDC_R4	n/a	Alternate Function Pu	No pull-up and no pull	Low	LCD_R4 [RK043FN48	<b>V</b>
					Alternate Eurotian Du	No pull-up and no pull	Low	LCD R5 [RK043FN48	<b>~</b>
		PJ4	LTDC_R5	n/a					
			LTDC_R5 LTDC_R6	n/a n/a		No pull-up and no pull		LCD_R6 [RK043FN48	
		PJ4			Alternate Function Pu		Low		

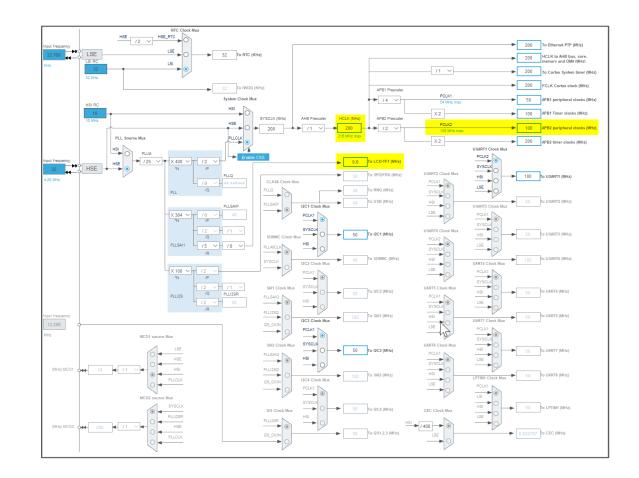


- 3. Framebuffer in internal RAM
  - Do
    - Parallel RGB Displays
      - Setup framebuffer in internal RAM
      - Configure the GPIO connections to the display
      - Configure the LTDC controller
      - Configure the LTDC pixel clock
      - Setting the framebuffer address
      - Check the framerate

~ Ø		LTDC Mode and Configuration	
ategories A->Z		Mode	
	Display Type RGB888 (24 bits)		~
System Core >			
Analog >			
Timers >			
Connectivity >		Configuration	
Multimedia 🗸	Reset Configuration		
٠			
	📀 Parameter Settings 🛛 🥺 Layer Settings 🔄 User Constants 🖉 NVIC Sett	ngs 🛛 🔮 GPIO Settings	
✓ DMA2D	Configure the below parameters :		
HDMI_CEC	Q Search (CrtI+F) ③ ④		0
Ø I2S1			U U
Ø 12S2	✓ Number of Layers		
Ø 12S3	Number of Layers V Windows Position	1 layer	
V LTDC			
A SAI2	Layer 0 - Window Horizontal Start	0	
	Layer 0 - Window Horizontal Stop	480	
	Layer 0 - Window Vertical Start	0	
	Layer 0 - Window Vertical Stop	272	
Security >	V Pixel Parameters		
Security /	Layer 0 - Pixel Format	RGB565	
Computing >	✓ Blending	0.55	
oomputing	Layer 0 - Alpha constant for blending	255	
Middleware >	Layer 0 - Default Alpha value	0	
inadionaro	Layer 0 - Blending Factor1	Alpha constant x Pixel Alpha	
Application >	Layer 0 - Blending Factor2	Alpha constant x Pixel Alpha	
, deprivation	V Frame Buffer		
	Layer 0 - Color Frame Buffer Start Adress	0xC000000	
	Layer 0 - Color Frame Buffer Line Length (Image Width)	480	
	Layer 0 - Color Frame Buffer Number of Lines (Image Height)	272	
	V BackGround Color		
	Layer 0 - Blue	0	
	Layer 0 - Green	0	
	Layer 0 - Red	0	



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  - Do
    - Parallel RGB Displays
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      - Configure the LTDC pixel clock
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### • 3. Framebuffer in internal RAM

- Do
  - Parallel RGB Displays
    - Setup framebuffer in internal RAM
    - Configure the GPIO connections to the display
    - Configure the LTDC controller
    - Configure the LTDC pixel clock
    - Setting the framebuffer address
    - Check the framerate

#### main.c

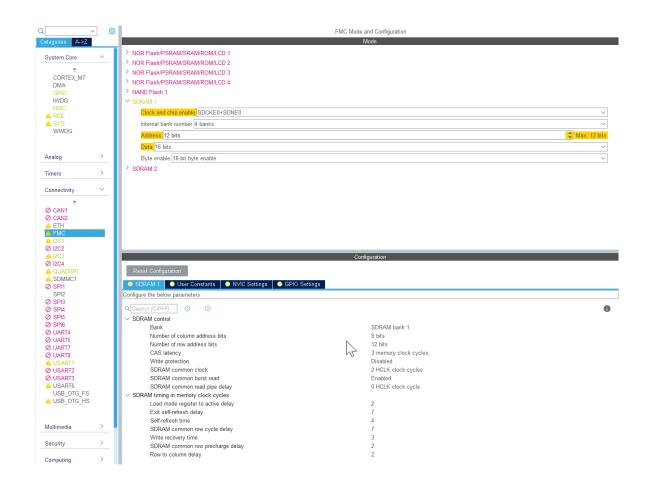
/\* USER CODE BEGIN 2 \*/
HAL\_LTDC\_SetAddress(&hltdc, framebuffer, LTDC\_LAYER\_1);
/\* USER CODE END 2 \*/



### • 4. External Ram

### Motivation

- External RAM is often required since the framebuffer(s) does not fit in internal RAM
- Goal
  - Enable External RAM and be able to r/w
- Prerequisites
  - Information about the RAM
  - Information about connection between the MCU and RAM
- Do
  - Setup in STM32CubeMX
  - Some RAMs needs extra C code





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tegories A->Z	۰			FMC Mode and Mod				
egones Aevz	-			Widu	ue			
vstem Core 🗸 🗸		RAM/SRAM/ROM/LCD 1						
<i>,</i>	<ul> <li>NOR Flash/PS</li> </ul>	RAM/SRAM/ROM/LCD 2						
÷	NOR Flash/PS	RAM/SRAM/ROM/LCD 3						
CORTEX_M7 DMA	> NOR Flash/PS	RAM/SRAM/ROM/LCD 4						
GPIO	> NAND Flash 1							
IWDG	Y SDRAM 1							
NVIC		hip enable SDCKE0+SDN	IEA					
RCC								
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mers >	> SDRAM 2							
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FMC 12C1 12C2 12C3	Search (CrtI+F) Pin Name	Signal on Pin				Maximum output speed	User Label	Modified
FMC 12C1 12C2 12C3 12C4	Search (Crt/+F) Pin Name  PE12	FMC_D9	n/a	Alternate Function Pu N	to pull-up and no pull	Very High	User Label FMC_D9 [MT48LC4M	Modified
FMC 12C1 12C2 12C3 12C4 QUADSPI	Search (CrtI+F) Pin Name PE12 PE13	FMC_D9 FMC_D10	n/a n/a	Alternate Function Pu N Alternate Function Pu N	to pull-up and no pull to pull-up and no pull	Very High Very High	User Label FMC_D9 [MT48LC4M FMC_D10 [MT48LC4	Modified V
FMC 12C1 12C2 12C3 12C4 QUADSPI SDMMC1	Search (CrtH+F) Pin Name * PE12 PE13 PE14	FMC_D9 FMC_D10 FMC_D11	n/a n/a n/a	Alternate Function Pu N Alternate Function Pu N Alternate Function Pu N	to pull-up and no pull to pull-up and no pull to pull-up and no pull	Very High Very High Very High	User Label FMC_D9 [MT48LC4M FMC_D10 [MT48LC4 FMC_D11 [MT48LC4	Modified V V
FMC 12C1 12C2 12C3 12C4 QUADSPI SDMMC1	Search (Citl+F) Pin Name * PE12 PE13 PE14 PE15	FMC_D9 FMC_D10 FMC_D11 FMC_D12	n/a n/a n/a	Alternate Function Pu N Alternate Function Pu N Alternate Function Pu N Alternate Function Pu N	to pull-up and no pull to pull-up and no pull to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High	User Label FMC_D9 [MT48LC4M FMC_D10 [MT48LC4 FMC_D11 [MT48LC4 FMC_D12 [MT48LC4	Modified V V
FMC 12C1 12C2 12C3 12C4 QUADSPI SDMMC1 SPI1 SPI2	Search (CritHF) PE12 PE13 PE14 PE15 PF0	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0	n/a n/a n/a n/a n/a	Alternate Function Pu., N. Alternate Function Pu., N. Alternate Function Pu., N. Alternate Function Pu., N. Alternate Function Pu., N.	to pull-up and no pull to pull-up and no pull to pull-up and no pull to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High	User Label FMC_D9 (MT48LC4M FMC_D10 (MT48LC4 FMC_D11 (MT48LC4 FMC_D12 (MT48LC4 FMC_A0 (MT48LC4M	Modified V V V
FMC 12C1 12C3 12C3 12C4 QUADSPI SDIMC1 SPI1 SPI2 SPI3	Search (CrtH+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A1	n/a n/a n/a	Alternate Function Pu., N. Alternate Function Pu., N.	to pull-up and no pull to pull-up and no pull to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High	User Label FMC_D9 (MT48LC4M FMC_D10 (MT48LC4 FMC_D11 (MT48LC4 FMC_D12 (MT48LC4M FMC_A0 (MT48LC4M FMC_A1 (MT48LC4M	Modified V V V
FMC 2C1 2C2 2C2 2C2 2C2 2C4 2C4 2UADSPI SDMMC1 SPI1 SPI2 SPI2 SPI3 SPI4 SPI4 SPI5 SPI5 SPI5 SPI5 SPI5 SPI5 SPI5 SPI5	Search (CritH+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A1 FMC_A2	n/a n/a n/a n/a n/a	Alternate Function Pu N Alternate Function Pu N	lo pull-up and no pull lo pull-up and no pull	Very High Very High Very High Very High Very High Very High Very High	User Label FMC_D9 [MT48LC4M FMC_D10 [MT48LC4 FMC_D11 [MT48LC4 FMC_D12 [MT48LC4M FMC_A0 [MT48LC4M FMC_A1 [MT48LC4M FMC_A2 [MT48LC4M	Modified V V V V V V
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FMC 2C1 2C2 2C2 2C2 2C2 2C3 2C4 4 0005PI 5PI2 5PI3 5PI3 5PI5 5PI5 5PI6 5PI6 UART4	Search (Citt+F) PE12 PE13 PE14 PE15 PF0 PF1 PF2 PF3 PF3 PF4	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A0 FMC_A2 FMC_A3 FMC_A4	n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N. Alternate Function Pu., N.	to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High Very High Very High Very High	User Label FMC_09 [MT48LC4 FMC_010 [MT48LC4 FMC_011 [MT48LC4 FMC_012 [MT48LC4 FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A4 [MT48LC4M	Modified V V V V V V V V V V V V V
EMC 2021 2022 2023 2024 2	Search (Crit+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A1 FMC_A2 FMC_A3 FMC_A4 FMC_A4 FMC_A5	n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N Alternate Function Pu., N	to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High Very High Very High Very High	User Label           FMC_D9 [MT48LC4M           FMC_D10 [MT48LC4           FMC_D11 [MT48LC4           FMC_A0 [MT48LC4M           FMC_A1 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_MA [MT48LC4M           FMC_MA [MT48LC4M	Modified 2 2 2 2 2 2 2 2 2 2 2 2 2
EMC 2021 2023 2023 2024 QUADSPI SPN1 SP12 SP13 SP16 SP16 SP16 SP16 SP16 UART4 UART5 UART7	Search (Citt+F) PE12 PE13 PE14 PE15 PF0 PF1 PF2 PF3 PF3 PF4	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A0 FMC_A2 FMC_A3 FMC_A4	n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N Alternate Function Pu., N	to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High Very High Very High Very High Very High Very High	User Label FMC_09 [MT48LC4 FMC_010 [MT48LC4 FMC_011 [MT48LC4 FMC_012 [MT48LC4 FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A4 [MT48LC4M	Modified C C C C C C C C C C C C C
FMC 2021 2022 2023 2024 2035 2040 5911 5914 5915 5915 5916 UART5 UART5 UART75 UART75 UART75	Search (Crit+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF11           PF12	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A1 FMC_A2 FMC_A3 FMC_A4 FMC_A4 FMC_A5	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N Alternate Function Pu., N	to pull-up and no pull to pull-up and no pull	Very High Very High Very High Very High Very High Very High Very High Very High Very High Very High	User Label           FMC_D9 [MT48LC4M           FMC_D10 [MT48LC4           FMC_D11 [MT48LC4           FMC_A0 [MT48LC4M           FMC_A1 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_A3 [MT48LC4M           FMC_MA [MT48LC4M           FMC_MA [MT48LC4M	Modified C C C C C C C C C C C C C
EMC 2021 2022 2023 2024 2	Search (Cit/+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF111	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A1 FMC_A1 FMC_A2 FMC_A3 FMC_A3 FMC_A5 FMC_A5 FMC_SDNRAS	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N Alternate Function Pu., N	to pull-up and no pull to pull-up and no pull	Very High Very High	User Label FMC_D9 [MT48LC4M FMC_D10 [MT48LC4 FMC_D11 [MT48LC4 FMC_D12 [MT48LC4M FMC_A0 [MT48LC4M FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A4 [MT48LC4M FMC_A5 [MT48LC4M FMC_A5 [MT48LC4M FMC_SDNA5 [MT48 FMC_SDNA5 [MT48] FMC_SDNA5 [MT48 FMC_SDNA5 [MT48] FMC_SDNA5 [MT48] FMC	Modified C C C C C C C C C C C C C
FMC ) CC1 ) CC2 ) CC2 ) CC3 ) CC4 )	Search (Crit+F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF11           PF12	FMC_D9 FMC_D10 FMC_D11 FMC_D11 FMC_A0 FMC_A1 FMC_A3 FMC_A3 FMC_A3 FMC_A4 FMC_SDNRAS FMC_A6	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu., N Alternate Function Pu., N	to pull-up and no pull to pull-up and no pull	Very High Very High	User Label FMC_D9 (MT48LC4M FMC_D10 (MT48LC4 FMC_D11 (MT48LC4 FMC_D12 (MT48LC4M FMC_D4 (MT48LC4M FMC_A2 (MT48LC4M FMC_A2 (MT48LC4M FMC_A5 (MT48LC4M FMC_A5 (MT48LC4M	Modified C C C C C C C C C C C C C
FMC ICC1 ICC2 ICC3 ICC3 ICC4 I	Search (Crit+F)           Pin Name           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF11           PF2           PF3           PF4           PF5           PF12           PF13	FMC_D9 FMC_D10 FMC_D11 FMC_D11 FMC_A0 FMC_A4 FMC_A4 FMC_A3 FMC_A5 FMC_A5 FMC_SDNRAS FMC_A6 FMC_A6 FMC_A7	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu. N Alternate Function Pu. N	to pull-up and no pull to pull-up and no pull	Very High Very High	User Label FMC_09 [MT48LC4M FMC_D10 [MT48LC4 FMC_D11 [MT48LC4 FMC_D12 [MT48LC4M FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_A4 [MT48LC4M FMC_SDNRAS [MT48 FMC_SDNRAS [MT48 FMC_A6 [MT48LC4M FMC_A6 [MT48LC4M	Modified C C C C C C C C C C C C C C C C C C C
FMC ICC1 ICC2 ICC3 ICC3 ICC4 I	Search (CdH+F)           Pct Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF11           PF12           PF13           PF14	FMC_D9 FMC_D10 FMC_D11 FMC_D12 FMC_A0 FMC_A1 FMC_A3 FMC_A3 FMC_A5 FMC_SDNRAS FMC_A5 FMC_A5 FMC_A5 FMC_A7 FMC_A7 FMC_A8	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu. IN Alternate Function Pu. IN	to pull-up and no pull to pull-up and no pull	Very High	User Label FMC_D9 [MT48LC44, FMC_D10 [MT48LC4, FMC_D11 [MT48LC4, FMC_D12 [MT48LC44, FMC_A1 [MT48LC44, FMC_A2 [MT48LC444, FMC_A2 [MT48LC444, FMC_A3 [MT48LC444, FMC_A5 [MT48LC444, FMC_A5 [MT48LC444, FMC_A6 [MT48LC444, FMC_A7	Modified C C C C C C C C C C C C C
FMC AC1 DC2 DC3 DC4 SC3 DC4 SC4 SC4 SC4 SP1 SP1 SP1 SP1 SP1 SP1 SP1 SP1	Search (CdH+F) Po Name PE13 PE14 PE15 PF0 PF1 PF2 PF2 PF3 PF4 PF5 PF1 PF12 PF13 PF14 PF15	FMC_D9           FMC_D10           FMC_D11           FMC_D11           FMC_D12           FMC_A1           FMC_A2           FMC_A3           FMC_A5           FMC_A5           FMC_A6           FMC_A6           FMC_A6           FMC_A7           FMC_A8           FMC_A8           FMC_A8           FMC_A8           FMC_A8           FMC_A8           FMC_A8           FMC_A8	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu. IN Alternate Function Pu. N Alternate Function Pu. N	lo pull-up and no pull lo pull-up and no pull	Very High	User Label FAIC_DPI(MT48LC4, FMC_DT9(MT48LC4, FMC_DT9(MT48LC4, FMC_DT9(MT48LC4, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A7(MT48LC4M, FMC_A8(MT48	Modified C C C C C C C C C C C C C
FMC AC1 DC2 DC3 DC4 SC3 DC4 SC4 SC4 SC4 SP1 SP1 SP1 SP1 SP1 SP1 SP1 SP1	Bearch (Cdf#F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF1           PF5           PF11           PF12           PF13           PF14           PF15           PG0	FMC_D9           FMC_D10           FMC_D11           FMC_D12           FMC_A1           FMC_A2           FMC_A3           FMC_A3           FMC_A3           FMC_A5           FMC_A5           FMC_A5           FMC_A5           FMC_A5           FMC_A6           FMC_A6           FMC_A7           FMC_A8           FMC_A10	n/a n/a n/a n/a n/a n/a n/a n/a n/a n/a	Alternate Function Pu. IN Alternate Function Pu. IN	lo pull-up and no pull lo pull-up and no pull	Very High	User Labol FMC, DD (MT48LCA, FMC, DT0 (MT48LCA, FMC, DT1 (MT48LCA, FMC, DT1 (MT48LCA, FMC, DT1 (MT48LCM, FMC, AN (MT48LCM, FMC, AS (MT48LCM,	Modified 2 2 3 3 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5
FMC AC1 DC2 DC3 DC4 SC3 DC4 SC4 SC4 SC4 SP1 SP1 SP1 SP1 SP1 SP1 SP1 SP1	Search (CdI+F) Pin Name PE12 PE13 PE15 PF0 PF1 PF2 PF3 PF4 PF5 PF11 PF12 PF13 PF14 PF15 PF15 PG00 PG1	FINC, D9 FINC, D10 FINC, D11 FINC, D12 FINC, A0 FINC, A0 FINC, A0 FINC, A2 FINC, A4 FINC, A5 FINC, A6 FINC, A6 FINC, A6 FINC, A6 FINC, A6 FINC, A6 FINC, A6 FINC, A6 FINC, A1 FINC, A10 FINC, A20 FINC, A10 FINC, A20 FINC, A10 FINC, A20 FINC, A20 FI	nia nia nia nia nia nia nia nia nia nia	Alternate Function Pu. IN Alternate Function Pu. N Alternate Function Pu. N	Le guilt-up and ne pult- io pull-up and ne pult- lio pull-up and ne pult- lio pull-up and ne pult- lio pult-up and ne pult-	Very High	User Label FMC_DD [MT48LC4 FMC_DT0 [MT48LC4 FMC_DT0 [MT48LC4 FMC_DT0 [MT48LC4 FMC_A0 [MT48LC4M FMC_A2 [MT48LC4M FMC_340 [MT48LC4M]] FMC_340 [MT48LC4M FMC_340 [MT48LC4M]] FMC_340 [MT48L	Modified 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
FMC         AC1           AC1         AC1           CC3         CC3           D CC3         SCM           D CC4         SOMAC1           S SP1         SP2           S P1         SP2           S P1         SP2           S P1         SP3           S P1         SP4           S P1         SP4           S P1         SP4           S P4         SP4           S P4         SP4           S P45         UART5           S UART5         USART2           S USART2         USART3           USA_CT5_HS         USART5_S	Search (CdI+F) Po Name - Pe13 Pe14 Pe15 Pe16 Pe1 Pe1 Pe2 Pe3 Pe4 Pe5 Pe11 Pe12 Pe13 Pe4 Pe5 Pe11 Pe12 Pe13 Pe14 Pe15 Pe00 Pe10 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe2 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3	FINC. DB FINC. D10 FINC. D11 FINC. D12 FINC. A1 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A4 FINC. A4 FINC. A6 FINC. A7 FINC. A9 FINC. A1 FINC. A9 FINC. A11 FINC. BA1	na na na na na na na na na na na na na n	Alternate Function Pu. IN Alternate Function Pu. IN	lo pull-up and no pull- lo pull-up and no pull-	Very High	User Label FMC_D0 [MT48LCAH FMC_D10 [MT48LCAH FMC_D10 [MT48LCA FMC_D10 [MT48LCAH FMC_D10 [MT48LCAH FMC_D10 [MT48LCAH FMC_D10 [MT48LCAH FMC_A1 [MT48LCAH FMC_A5 [MT48LCAH	Modified C C C C C C C C C C C C C C C C C C C
FMC         AC1           AC1         AC1           CC3         CC3           D CC3         SCM           D CC4         SOMAC1           S SP1         SP2           S P1         SP2           S P1         SP2           S P1         SP3           S P1         SP4           S P1         SP4           S P1         SP4           S P4         SP4           S P4         SP4           S P45         UART5           S UART5         USART2           S USART2         USART3           USA_CT5_HS         USART5_S	Bearch (Cdf#F)           Pin Name           PE12           PE13           PE14           PE15           PF0           PF1           PF2           PF3           PF4           PF5           PF19           PF19           PF19           PF2           PF3           PF4           PF5           PF12           PF13           PF14           PF15           PG0           PG1           PG4           PG5           PG8	FINC, DB FINC, D10 FINC, D12 FINC, D12 FINC, A0 FINC, A0 FINC, A0 FINC, A2 FINC, A2 FINC, A4 FINC, A5 FINC, A6 FINC, A6 FINC, A7 FINC, A7 FINC, A9 FINC, A10 FINC, BA1 FINC, A3 FINC, A5 FINC, A5 FIN	na na na na na na na na na na na na na n	Alternate Function Pu. IN Alternate Function Pu. IN	Le guilt-up and ne pult- le pult-up and ne pult-	Very High           Very High	User Label FMC_DD [MT48LC4 FMC_DT0 [MT48LC4 FMC_DT0 [MT48LC4 FMC_DT0 [MT48LC4 FMC_A1 [MT48LC4 FMC_A2 [MT48LC4M FMC_A2 [MT48LC4M FMC_32 [MT48LC4M FMC_33 [MT48LC4M] [MT48LC4M FMC_33 [MT48LC4M]	Modified         C           C         C         C
<ul> <li>SPI3</li> <li>SPI3</li> <li>SPI6</li> <li>SPI6</li> <li>UART4</li> <li>UART5</li> <li>UART5</li> <li>UART6</li> <li>USART1</li> <li>USART2</li> <li>USART3</li> <li>USART3</li> <li>USART6</li> <li>USB_OTG_FS</li> <li>USB_OTG_HS</li> </ul>	Search (CdI+F) Po Name - Pe13 Pe14 Pe15 Pe16 Pe1 Pe1 Pe2 Pe3 Pe4 Pe5 Pe11 Pe12 Pe13 Pe4 Pe5 Pe11 Pe12 Pe13 Pe14 Pe15 Pe00 Pe10 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe12 Pe13 Pe14 Pe2 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3 Pe3	FINC. DB FINC. D10 FINC. D11 FINC. D12 FINC. A1 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A3 FINC. A4 FINC. A4 FINC. A6 FINC. A7 FINC. A9 FINC. A1 FINC. A1 FINC. A1 FINC. B4 FINC. B41	na na na na na na na na na na na na na n	Alternate Function Pu. IN Alternate Function Pu. IN	Lo pull-up and no pull- bo pull-up and no pull-	Very High	User Label FMC_D0 [MT48LCAH FMC_D10 [MT48LCAH FMC_D10 [MT48LCA FMC_D11 [MT48LCA FMC_D12 [MT48LCAH FMC_D12 [MT48LCAH FMC_D14 [MT48LCAH FMC_A1 [MT48LCAH FMC_A5 [MT48LCAH	

FMC_SDRAM_CommandTypeDef(	command;	
Command.CommandMode	= FMC_SDRAM_CMD_CLK_ENABLE;	
Command.CommandTarget	= FMC_SDRAM_CMD_TARGET_BANK1;	
Command.AutoRefreshNumber		
Command.ModeRegisterDefini	tion = 0;	



### • 4. External Ram

- Motivation
  - External RAM is often required since the framebuffer(s) does not fit in internal RAM
- Goal
  - Enable External RAM and be able to r/w
- Prerequisites
  - Information about the RAM
  - Information about connection between the MCU and RAM
- Do
  - Setup in STM32CubeMX
  - Some RAMs needs extra C code

/* FMC SDRAM control configuration	*/	
SdramHandle.Init.SDBank	=	FMC_SDRAM_BANK2;
/* Row addressing: [7:0] */		
SdramHandle.Init.ColumnBitsNumber	=	FMC_SDRAM_COLUMN_BITS_NUM_8;
/* Column addressing: [11:0] */		
SdramHandle.Init.RowBitsNumber	=	<pre>FMC_SDRAM_ROW_BITS_NUM_12;</pre>
SdramHandle.Init.MemoryDataWidth	=	SDRAM_MEMORY_WIDTH;
SdramHandle.Init.InternalBankNumber	=	FMC_SDRAM_INTERN_BANKS_NUM_4;
SdramHandle.Init.CASLatency	=	SDRAM_CAS_LATENCY;
SdramHandle.Init.WriteProtection	=	<pre>FMC_SDRAM_WRITE_PROTECTION_DISABLE;</pre>
SdramHandle.Init.SDClockPeriod	=	SDCLOCK_PERIOD;
SdramHandle.Init.ReadBurst	=	SDRAM_READBURST;
SdramHandle.Init.ReadPipeDelay	=	<pre>FMC_SDRAM_RPIPE_DELAY_1;</pre>
Manuary 1		

/* SDRAM controller init	Memory 1					×
/*weak function can b		d0000000 ~	Memory16	~	. t. 就	
BSP_SDRAM_MspInit(&Sdram	Oxefffff	90				•
<b>if</b> (HAL_SDRAM_Init(&Sdram	0xcfffff					6
{	0xcfffff					
sdramstatus = SDRAM ERI	0xcfffff	c0				
-	0xcfffff	d0				
else	0xcfffff	e0				
erse	0xcfffff	f0				
{	0xd00000	00 12345678	87654321	ABCDABCO	00000000	
sdramstatus = SDRAM OK	0xd00000	10 00000000	00000000	00000000	00000000	
}	0xd00000	20 00000000	00000000	00000000	00000000	
J	0xd00000	30 00000000	00000000	00000000	00000000	
	0xd00000	40 00000000	00000000	00000000	00000000	
/* SDRAM initialization	0xd00000	50 00000000	00000000	00000000	00000000	
BSP SDRAM Initialization	0xd00000		000000000	000000000	000000000	
	0xd00000	70 00000000	00000000	00000000	00000000	
return sdramstatus;	0xd00000			00000000	00000000	¥
}						

uint32\_t \*externalRAM = 0xC000000; const uint32\_t size = 1000; //write external RAM for(int i = 0; i < size; i++)

externalRAM[i] = i;



- 5. Framebuffer in external RAM
  - Motivation
    - Getting graphics on the display from External RAM
  - Goal
    - Remove Framebuffer from Internal RAM, and have the Framebuffer in external RAM
  - Prerequisites
    - Address of the framebuffer in the external RAM
  - Do
    - Place the framebuffer in external RAM
    - Setup the display controller to read from the external RAM

#### main.c

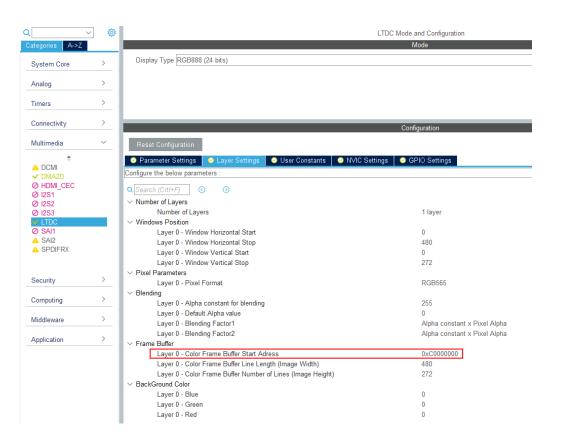
uint16\_t\* framebuffer = (uint16\_t\*)0xC0000000; //16 bpp framebuffer

#### main.c

/\* USER CODE BEGIN 2 \*/
HAL\_LTDC\_SetAddress(&hltdc, framebuffer, LTDC\_LAYER\_1);
/\* USER CODE END 2 \*/



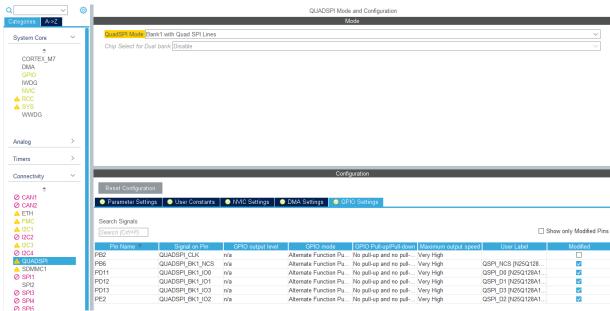
- 5. Framebuffer in external RAM
  - Motivation
    - Getting graphics on the display from External RAM
  - Goal
    - Remove Framebuffer from Internal RAM, and have the Framebuffer in external RAM
  - Prerequisites
    - Address of the framebuffer in the external RAM
  - Do
    - Place the framebuffer in external RAM
    - Setup the display controller to read from the external RAM





- 6. External addressable flash
  - Motivation
    - External Flash memory is often needed in graphic application since it consist of a lot of images.
  - Goal
    - Enable external flash In memory mapped mode and read data from it.
  - Prerequisites
    - Information about the flash
    - Information about connection between the MCU and flash
  - Do
    - Setup in CubeMX

Setup Memory Mapped mode in code



### 6. External addressable flash

- Motivation
  - External Flash memory is often needed in ٠ graphic application since it consist of a lot of images.
- Goal
  - Enable external flash In memory mapped mode • and read data from it.
- Prerequisites
  - Information about the flash •
  - Information about connection between the • MCU and flash
- Do
  - Setup in CubeMX

Setup Memory Mapped mode in code life auamenter

#### main.c

QSPI CommandTypeDef s command: QSPI MemoryMappedTypeDef s mem mapped cfg;

_command.InstructionMode	QSPI_INS
_command.Instruction	QUAD_INC
_command.AddressMode	QSPI_ADD
_command.AddressSize	QSPI_ADD
_command.AlternateByteMode	QSPI_ALT
_command.DataMode	QSPI_DAT
_command.DummyCycles	N25Q128A
_command.DdrMode	QSPI_DDF
_command.DdrHoldHalfCycle	QSPI_DDF
_command.SIOOMode	QSPI_SIC

OUT FAST READ CMD; DRESS 4 LINES;

STRUCTION 1 LINE;

- DRESS\_24\_BITS;
- FERNATE BYTES NONE;
- A 4 LINES;
- DUMMY CYCLES READ QUAD;
- MODE DISABLE;
- HHC ANALOG DELAY; OO INST EVERY CMD;

s\_mem\_mapped\_cfg.TimeOutActivation = QSPI\_TIMEOUT\_COUNTER\_DISABLE;

if (HAL QSPI MemoryMapped(&QSPIHandle, &s command, &s mem mapped cfg) != HAL OK)

return QSPI ERROR;

- 6. External addressable flash
  - Motivation
    - External Flash memory is often needed in graphic application since it consist of a lot of images.
  - Goal
    - Enable external flash In memory mapped mode and read data from it.
  - Prerequisites
    - Information about the flash
    - Information about connection between the MCU and flash
  - Do
    - Setup in CubeMX

Setup Memory Mapped mode in code



- 7. External flash in block mode
  - Motivation
    - Non-Memory-Mapped Flash memory requires a driver to work with TouchGFX
  - Goal
    - A driver that can read from a location in the flash memory and store it in an array.
  - Prerequisites
    - Information about the flash
    - Information about connection between the MCU and flash
    - The flash speed



- 7. External flash in block mode
  - Do
    - Configure the NAND flash via STM32CubeMX via the FMC
    - Set the QSPI flash, similar to memory-mapped
      - Including GPIO
    - Add code to read from an address of the flash

Pinout & Configura	ation	Clock Configuration	Project
		Additional Software 🔹 💊	Pinout
Q 🔕		FMC Mode and Configuration	
Categories A->Z		Mode	
Connectivity ~	> NOR Flash/PS	RAM/SRAM/ROM/LCD 1	
<u>.</u>	> NOR Flash/PS	RAM/SRAM/ROM/LCD 2	
FDCAN1	> NOR Flash/PS	RAM/SRAM/ROM/LCD 3	
FDCAN2	> NOR Flash/PS	RAM/SRAM/ROM/LCD 4	
FMC I2C1	✓ NAND Flash 1		
1201		nip Select	
12C3	Data/Addre	ss Disable	$\sim$
✓ I2C4 LPUART1	Ready or b	usy Disable	~
MDIOS	> SDRAM 1		
OCTOSPI1     OCTOSPI2	> SDRAM 1		





- 8. Hardware acceleration
  - Motivation
    - The Chrom-ART (DMA2D), has the possibility to drastically improving the graphical performance by transferring data from memory into the framebuffer
  - Goal
    - Enable Chrom-ART and read and write data using it
  - Prerequisites
    - MCU with Chrom-ART
  - Do

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- Setup Chrom-ART in STM32CubeMX
- Add code to fil a specific color in a rectangle in target memory

Pinout &	Configurati	ion Clo	ck Configuration
		Ad	ditional Software Vino
<b>ک</b> ا	0	DMA2D Mo	de and Configuration
Categories A->Z			Mode
System Core	>	Activated	
Analog	>		
Timers	>	Co	nfiguration
		Reset Configuration	
Connectivity		😔 Parameter Settings 🛛 😔 User Consta	ants 🛛 😔 NVIC Settings
Multimedia	~	Configure the below parameters :	
÷		Q Search (CrtI+F) ③ ③	0
DCMI V DMA2D	_	✓ Basic Parameters	
GFXMMU	_	Transfer Mode	Memory to Memory
HDMI_CEC		Color Mode	RGB565
I2S1		Output Offset	
I2S2		DMA2D Bytes Swap DMA2D Line Offset Mode	Bytes in regular order in output FIFO
12S3 12S6			Line offsets expressed in pixels
JPEG		<ul> <li>Foreground layer Configuration</li> <li>DMA2D Input Color Mode</li> </ul>	RGB565
✓ LTDC		DMA2D ALPHA MODE	
PSSI			No modification of the alpha channel value 0
SAI1		Input Alpha Input Offset	0
SAI2		DMA2D ALPHA Inversion	u Regular Alpha
SPDIFRX		DMA2D ALPHA Inversion DMA2D Red and Blue swap	Regular Alpha Regular mode (RGB or ARGB)
			A No chroma sub-sampling 4:4:4

- 8. Hardware acceleration
  - Motivation
    - The Chrom-ART (DMA2D), has the possibility to drastically improving the graphical performance by transferring data from memory into the framebuffer
  - Goal
    - Enable Chrom-ART and read and write data using it
  - Prerequisites
    - MCU with Chrom-ART
  - Do

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- Setup Chrom-ART in STM32CubeMX
- Add code to fil a specific color in a rectangle in target memory

Pinout &	Configurat	tion Clock Configurati	on	
~	0	NVIC Mode and Configuration		
ategories A->Z		Configuration		
System Core	~	Solution Solution		
		NVIC Interrupt Table	Enable	dPreem
€ BDMA1		Non maskable interrupt	$\checkmark$	0
BDMA2		Hard fault interrupt	~	0
CORTEX_M7		Memory management fault	~	0
DMA		Pre-fetch fault, memory access fault	~	0
GPIO		Undefined instruction or illegal state	~	0
IWDG1		System service call via SWI instruction	~	0
MDMA	_	Debug monitor	~	0
NVIC V RCC		Pendable request for system service	~	15
V SYS		System tick timer	~	15
WWDG1		PVD and PVM interrupts through EXTI line		5
		Flash global interrupt		5
		RCC global interrupt		5
Analog	>	EXTI line2 interrupt	~	5
Analog		Time base: TIM6 global interrupt, DAC1_CH1 and DAC1_CH	~	0
Timers	>	FPU global interrupt		5
		LTDC global interrupt	~	5
Connectivity	>	LTDC Error global Interrupt		5
,		DMA2D global interrupt		5
Multimedia	~	OCTOSPI1 global interrupt	~	5
		I2C4 event interrupt		5
\$		I2C4 error interrupt		5
V DMA2D		HSEM1 global interrupt		5
GEXMMU		ECC diagnostic Global Interrupt		5

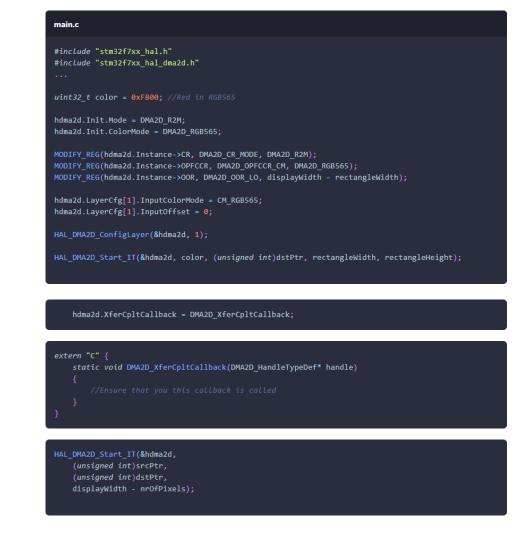
Pinout & C	onfigurat	ion	Clock Conf	iguration	Proje
			Additional S	oftware	✓ Pinout
~	٢		NVIC Mode	and Configuration	
ategories A->Z			Cor	nfiguration	
System Core	~	🥝 NVIC 🛛 😔 Code generation			
\$		Enabled interrupt table Memory management fault	Select for i	Generate IRQ handler	Call HAL handler
BDMA1		Pre-fetch fault, memory access fault		✓	
BDMA2		Undefined instruction or illegal state		✓	
CORTEX_M7		System service call via SWI instruc			
DMA		Debug monitor		✓	
GPIO IWDG1		Pendable request for system service			
MDMA		System tick timer			
NVIC		EXTI line2 interrupt		✓	✓
RCC		Time base: TIM6 global interrupt, D		✓	✓
SYS		LTDC global interrupt		✓	✓
WWDG1		DMA2D global interrupt		✓	✓
		OCTOSPI1 global interrupt		✓	✓

### • 8. Hardware acceleration

- Motivation
  - The Chrom-ART (DMA2D), has the possibility to drastically improving the graphical performance by transferring data from memory into the framebuffer
- Goal
  - Enable Chrom-ART and read and write data using it
- Prerequisites
  - MCU with Chrom-ART
- Do

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- Setup Chrom-ART in STM32CubeMX
- Add code to fil a specific color in a rectangle in target memory

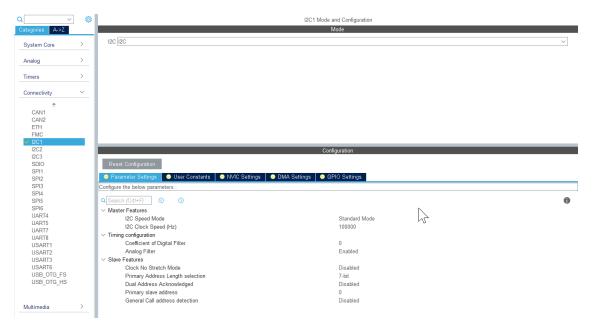


### • 9. Touch Controller

- Motivation
  - Setting up the Touchcontroller, enables the users to interact with the application
- Goal
  - Touch coordinates can be read from the touch controller
- Prerequisites
  - Display with a touch controller
  - Drivers to read from the touch controller
- Do
  - Setup the communication with the touch controller



Driver code for touch controller communication

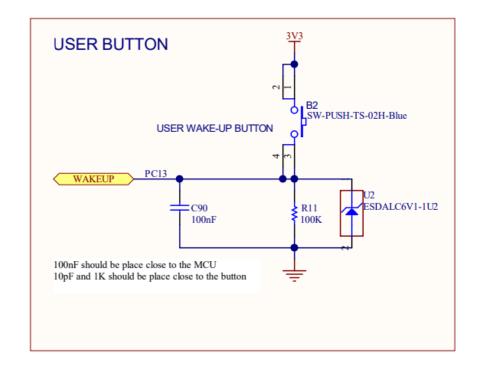




- 10. Physical Buttons
  - Motivation
    - Physical buttons can function as an external events to interact with the application, or as an alternative to touch
  - Goal
    - Setup the application to receive input from a button
  - Prerequisites
    - Physical button connected to MCU
  - Do

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- Setup the GPIO for the button in STMCubeMX32
- Add code to react on the GPIO



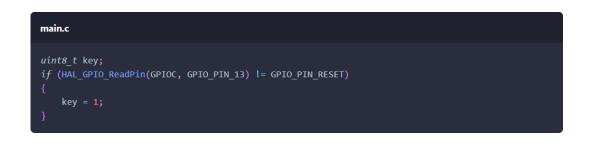
### • 10. Physical Buttons

- Motivation
  - Physical buttons can function as an external events to interact with the application, or as an alternative to touch
- Goal
  - Setup the application to receive input from a button
- Prerequisites
  - Physical button connected to MCU
- Do

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- Setup the GPIO for the button in STMCubeMX32
- Add code to react on the GPIO

PA2       n/a       Low       Output Pu       Pull-up       Low       n/a       LCD_ON/       Image: Comparison of the	PA2 n/a Low Output Pu Pull-up Low n/a LCD	
PB14       n/a       Low       Output Pu       No pull-up       Low       n/a       RENDER       Image: Comparison of the comparison	PA12 n/a Low Output Pu No pull-up Low n/a VSN	
PB15       n/a       Low       Output Pu       No pull-up       Low       n/a       FRAME_R       Image: Comparison of the comparison		NC_F 🔽
PC13 n/a n/a Input mode Pull-down n/a n/a BTN_USER PG2 n/a Low Output Pu No pull-up Low n/a LED2	PB14 n/a Low Output Pu No pull-up Low n/a REM	DER 🔽
PG2 n/a Low Output Pu No pull-up Low n/a LED2 🗹	PB15 n/a Low Output Pu No pull-up Low n/a FRA	ME_R 🔽
	PC13 n/a n/a Input mode Pull-down n/a n/a BTN	USER 🔽
DO11 a/a Law Output Du Na sullium Law a/a LED2	PG2 n/a Low Output Pu No pull-up Low n/a LED	2
		2
PC13 Configuration :	PG11 n/a Low Output Pu No pull-up Low n/a LEP PC13 Configuration :	



- 11. Flash Loader
  - Motivation
    - Enable the solution to write data to the external flash when programming
  - Goal
    - Select a mechanism for loading data to the external flash
  - Prerequisites
    - Information about the flash
    - Information about connection between the MCU and flash
  - Do

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- Flash loader for STM32CubeProgrammer
- Proprietary application-based solution

### Where to go next?

- More information can be found in documentation: Hardware Selection & Board Bring Up
- To get started with the Abstraction Layer Development, read the <u>TouchGFX AL Development Introduction</u>
- Or watch the presentation

**Abstraction Layer Development - Introduction** 



# Thank you

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